1. **Netlists**
2. NETLIST FOR ADD/SUB

simulator lang=spectre

global 0 vdd!

include "/net/plato.ee.Virginia.EDU/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_ff/NMOS\_VTL.inc"

include "/net/plato.ee.Virginia.EDU/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_ff/PMOS\_VTL.inc"

// Cell name: ece3663Inverter

// An inverter with sizing parameters and parameterized AD,AS,PD,PS

// The S/D parameters assume a single-finger device

subckt ece3663Inverter VDD VSS in out

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MP (out in VDD VDD) PMOS\_VTL w=wp l=lp as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

MN (out in VSS VSS) NMOS\_VTL w=wn l=ln as=100n\*wn ad=100n\*wn ps=200n+wn pd=200n+wn m=mult

ends ece3663Inverter

// End of subcircuit definition

// Cell name: TransmissionGate

// View name: schematic

subckt TransmissionGate VDD VSS In PmosG NmosG Out

parameters wp=180n wn=90n mult=1

M0 (In NmosG Out VSS) NMOS\_VTL w=wn l=ln as=100n\*2\*wn ad=100n\*2\*wn ps=200n+2\*wn pd=200n+2\*wn m=mult

M1 (In PmosG Out VDD) PMOS\_VTL w=wp l=lp as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

ends TransmissionGate

// End of subcircuit definition.

subckt inputBuffer in out

I0 (vdd! 0 in net0) ece3663Inverter

I1 (vdd! 0 net0 out) ece3663Inverter

ends inputBuffer

subckt outputLoad out

I0 (vdd! 0 out net0) ece3663Inverter wp=720n wn=360n

ends outputLoad

// Input buffers

ICS (inCiAdd CiAdd) inputBuffer

ICM (inCiSub CiSub) inputBuffer

IA0 (inA0 A0) inputBuffer

IA1 (inA1 A1) inputBuffer

IA2 (inA2 A2) inputBuffer

IA3 (inA3 A3) inputBuffer

IA4 (inA4 A4) inputBuffer

IA5 (inA5 A5) inputBuffer

IA6 (inA6 A6) inputBuffer

IA7 (inA7 A7) inputBuffer

IA8 (inA8 A8) inputBuffer

IA9 (inA9 A9) inputBuffer

IA10 (inA10 A10) inputBuffer

IA11 (inA11 A11) inputBuffer

IA12 (inA12 A12) inputBuffer

IA13 (inA13 A13) inputBuffer

IA14 (inA14 A14) inputBuffer

IA15 (inA15 A15) inputBuffer

IB0 (inB0 B0) inputBuffer

IB1 (inB1 B1) inputBuffer

IB2 (inB2 B2) inputBuffer

IB3 (inB3 B3) inputBuffer

IB4 (inB4 B4) inputBuffer

IB5 (inB5 B5) inputBuffer

IB6 (inB6 B6) inputBuffer

IB7 (inB7 B7) inputBuffer

IB8 (inB8 B8) inputBuffer

IB9 (inB9 B9) inputBuffer

IB10 (inB10 B10) inputBuffer

IB11 (inB11 B11) inputBuffer

IB12 (inB12 B12) inputBuffer

IB13 (inB13 B13) inputBuffer

IB14 (inB14 B14) inputBuffer

IB15 (inB15 B15) inputBuffer

OL0 (S0) outputLoad

OL1 (S1) outputLoad

OL2 (S2) outputLoad

OL3 (S3) outputLoad

OL4 (S4) outputLoad

OL5 (S5) outputLoad

OL6 (S6) outputLoad

OL7 (S7) outputLoad

OL8 (S8) outputLoad

OL9 (S9) outputLoad

OL10 (S10) outputLoad

OL11 (S11) outputLoad

OL12 (S12) outputLoad

OL13 (S13) outputLoad

OL14 (S14) outputLoad

OL15 (S15) outputLoad

OL16 (M0) outputLoad

OL17 (M1) outputLoad

OL18 (M2) outputLoad

OL19 (M3) outputLoad

OL20 (M4) outputLoad

OL21 (M5) outputLoad

OL22 (M6) outputLoad

OL23 (M7) outputLoad

OL24 (M8) outputLoad

OL25 (M9) outputLoad

OL26 (M10) outputLoad

OL27 (M11) outputLoad

OL28 (M12) outputLoad

OL29 (M13) outputLoad

OL30 (M14) outputLoad

OL31 (M15) outputLoad

OLcS (CoutAdd) outputLoad

OLcM (CoutSub) outputLoad

// Cell name: onebitFullAdder

// One-bit full adder subcircuit with parameterized AD,AS,PD,PS

subckt onebitFullAdder VDD VSS A B Ci S Co

//wcg: size multiplier of carry gate

//wcinv: size multiplier of carry inverter

//wsg: size multiplier of sum gate

//wsinv: size multiplier of sum inverter

parameters wp=180n wn=90n mult=1 wcg=2 wcinv=1 wsg=1 wsinv=1

// Carry gate

P0 (X A net0 VDD) PMOS\_VTL w=wp\*16/3\*wcg l=50n as=100n\*wp\*16/3\*wcg ad=100n\*wp\*16/3\*wcg ps=200n+wp\*16/3\*wcg pd=200n+wp\*16/3\*wcg m=mult

P1 (net0 B net1 VDD) PMOS\_VTL w=wp\*16/3\*wcg l=50n as=100n\*wp\*16/3\*wcg ad=100n\*wp\*16/3\*wcg ps=200n+wp\*16/3\*wcg pd=200n+wp\*16/3\*wcg m=mult

P2 (net1 A VDD VDD) PMOS\_VTL w=wp\*4\*wcg l=50n as=100n\*wp\*4\*wcg ad=100n\*wp\*4\*wcg ps=200n+wp\*4\*wcg pd=200n+wp\*4\*wcg m=mult

P3 (X Ci net1 VDD) PMOS\_VTL w=wp\*4\*wcg l=50n as=100n\*wp\*4\*wcg ad=100n\*wp\*4\*wcg ps=200n+wp\*4\*wcg pd=200n+wp\*4\*wcg m=mult

P4 (net1 B VDD VDD) PMOS\_VTL w=wp\*4\*wcg l=50n as=100n\*wp\*4\*wcg ad=100n\*wp\*4\*wcg ps=200n+wp\*4\*wcg pd=200n+wp\*4\*wcg m=mult

N0 (X Ci net2 VSS) NMOS\_VTL w=wn\*2\*wcg l=50n as=100n\*wn\*2\*wcg ad=100n\*wn\*2\*wcg ps=200n+wn\*2\*wcg pd=200n+wn\*2\*wcg m=mult

N1 (net2 A VSS VSS) NMOS\_VTL w=wn\*2\*wcg l=50n as=100n\*wn\*2\*wcg ad=100n\*wn\*2\*wcg ps=200n+wn\*2\*wcg pd=200n+wn\*2\*wcg m=mult

N2 (net2 B VSS VSS) NMOS\_VTL w=wn\*2\*wcg l=50n as=100n\*wn\*2\*wcg ad=100n\*wn\*2\*wcg ps=200n+wn\*2\*wcg pd=200n+wn\*2\*wcg m=mult

N3 (X A net3 VSS) NMOS\_VTL w=wn\*2\*wcg l=50n as=100n\*wn\*2\*wcg ad=100n\*wn\*2\*wcg ps=200n+wn\*2\*wcg pd=200n+wn\*2\*wcg m=mult

N4 (net3 B VSS VSS) NMOS\_VTL w=wn\*2\*wcg l=50n as=100n\*wn\*2\*wcg ad=100n\*wn\*2\*wcg ps=200n+wn\*2\*wcg pd=200n+wn\*2\*wcg m=mult

//Carry out inverter

INV0 (VDD VSS X Co) ece3663Inverter wn=wn\*wcinv wp=wp\*wcinv

//Sum gate

P5 (Y X net4 VDD) PMOS\_VTL w=wp\*4/3\*wsg l=50n as=100n\*wp\*4/3\*wsg ad=100n\*wp\*4/3\*wsg ps=200n+wp\*4/3\*wsg pd=200n+wp\*4/3\*wsg m=mult

P6 (net4 Ci VDD VDD) PMOS\_VTL w=wp\*4\*wsg l=50n as=100n\*wp\*4\*wsg ad=100n\*wp\*4\*wsg ps=200n+wp\*4\*wsg pd=200n+wp\*4\*wsg m=mult

P7 (net4 A VDD VDD) PMOS\_VTL w=wp\*4\*wsg l=50n as=100n\*wp\*4\*wsg ad=100n\*wp\*4\*wsg ps=200n+wp\*4\*wsg pd=200n+wp\*4\*wsg m=mult

P8 (net4 B VDD VDD) PMOS\_VTL w=wp\*4\*wsg l=50n as=100n\*wp\*4\*wsg ad=100n\*wp\*4\*wsg ps=200n+wp\*4\*wsg pd=200n+wp\*4\*wsg m=mult

P9 (Y Ci net5 VDD) PMOS\_VTL w=wp\*36/5\*wsg l=50n as=100n\*wp\*36/5\*wsg ad=100n\*wp\*36/5\*wsg ps=200n+wp\*36/5\*wsg pd=200n+wp\*36/5\*wsg m=mult

P10 (net5 B net6 VDD) PMOS\_VTL w=wp\*36/5\*wsg l=50n as=100n\*wp\*36/5\*wsg ad=100n\*wp\*36/5\*wsg ps=200n+wp\*36/5\*wsg pd=200n+wp\*36/5\*wsg m=mult

P11 (net6 A net4 VDD) PMOS\_VTL w=wp\*36/5\*wsg l=50n as=100n\*wp\*36/5\*wsg ad=100n\*wp\*36/5\*wsg ps=200n+wp\*36/5\*wsg pd=200n+wp\*36/5\*wsg m=mult

N5 (Y X net7 VSS) NMOS\_VTL w=wn\*2\*wsg l=50n as=100n\*wn\*2\*wsg ad=100n\*wn\*2\*wsg ps=200n+wn\*2\*wsg pd=200n+wn\*2\*wsg m=mult

N6 (net7 A VSS VSS) NMOS\_VTL w=wn\*2\*wsg l=50n as=100n\*wn\*2\*wsg ad=100n\*wn\*2\*wsg ps=200n+wn\*2\*wsg pd=200n+wn\*2\*wsg m=mult

N7 (net7 B VSS VSS) NMOS\_VTL w=wn\*2\*wsg l=50n as=100n\*wn\*2\*wsg ad=100n\*wn\*2\*wsg ps=200n+wn\*2\*wsg pd=200n+wn\*2\*wsg m=mult

N8 (net7 Ci VSS VSS) NMOS\_VTL w=wn\*2\*wsg l=50n as=100n\*wn\*2\*wsg ad=100n\*wn\*2\*wsg ps=200n+wn\*2\*wsg pd=200n+wn\*2\*wsg m=mult

N9 (Y Ci net8 VSS) NMOS\_VTL w=wn\*3\*wsg l=50n as=100n\*wn\*3\*wsg ad=100n\*wn\*3\*wsg ps=200n+wn\*3\*wsg pd=200n+wn\*3\*wsg m=mult

N10 (net8 A net9 VSS) NMOS\_VTL w=wn\*3\*wsg l=50n as=100n\*wn\*3\*wsg ad=100n\*wn\*3\*wsg ps=200n+wn\*3\*wsg pd=200n+wn\*3\*wsg m=mult

N11 (net9 B VSS VSS) NMOS\_VTL w=wn\*3\*wsg l=50n as=100n\*wn\*3\*wsg ad=100n\*wn\*3\*wsg ps=200n+wn\*3\*wsg pd=200n+wn\*3\*wsg m=mult

//Sum inverter

INV1 (VDD VSS Y S) ece3663Inverter wn=wn\*wsinv wp=wp\*wsinv

ends onebitFullAdder

// End of subcircuit definition

subckt FA4 VDD VSS A0 A1 A2 A3 B0 B1 B2 B3 Ci S0 S1 S2 S3 Co

FA0 (VDD VSS A0 B0 Ci S0 Co0) onebitFullAdder

FA1 (VDD VSS A1 B1 Co0 S1 Co1) onebitFullAdder

FA2 (VDD VSS A2 B2 Co1 S2 Co2) onebitFullAdder

FA3 (VDD VSS A3 B3 Co2 S3 Co ) onebitFullAdder

ends FA4

//A-B = A + B' + Ci0 (Ci0 == 1)

// This works using two's complement. By inverting all the bits and adding a carry-in,

// B is converted to -B in two's complement representation. A and (-B) can then be

// added regularly

subckt onebitFullSub VDD VSS A B Ci S Co

I0 (VDD VSS B BNOT) ece3663Inverter

FS (VDD VSS A BNOT Ci S Co) onebitFullAdder

ends manchesterFS

subckt FS4 VDD VSS A0 A1 A2 A3 B0 B1 B2 B3 Ci S0 S1 S2 S3 Co

FA0 (VDD VSS A0 B0 Ci S0 Co0) onebitFullSub

FA1 (VDD VSS A1 B1 Co0 S1 Co1) onebitFullSub

FA2 (VDD VSS A2 B2 Co1 S2 Co2) onebitFullSub

FA3 (VDD VSS A3 B3 Co2 S3 Co ) onebitFullSub

ends manchesterFS4

// This uses separate circuits for ADD and SUB, which is unnecessary for the ALU

// However, it is simpler to construct and test with separate circuits

//ADD

FA0 (vdd! 0 A0 A1 A2 A3 B0 B1 B2 B3 CiAdd S0 S1 S2 S3 Co3S ) FA4

FA1 (vdd! 0 A4 A5 A6 A7 B4 B5 B6 B7 Co3S S4 S5 S6 S7 Co7S ) FA4

FA2 (vdd! 0 A8 A9 A10 A11 B8 B9 B10 B11 Co7S S8 S9 S10 S11 Co11S) FA4

FA3 (vdd! 0 A12 A13 A14 A15 B12 B13 B14 B15 Co11S S12 S13 S14 S15 CoutAdd) FA4

//SUB

FS0 (vdd! 0 A0 A1 A2 A3 B0 B1 B2 B3 CiSub M0 M1 M2 M3 Co3M ) FS4

FS1 (vdd! 0 A4 A5 A6 A7 B4 B5 B6 B7 Co3M M4 M5 M6 M7 Co7M ) FS4

FS2 (vdd! 0 A8 A9 A10 A11 B8 B9 B10 B11 Co7M M8 M9 M10 M11 Co11M) FS4

FS3 (vdd! 0 A12 A13 A14 A15 B12 B13 B14 B15 Co11M M12 M13 M14 M15 CoutSub) FS4

//Sources

V00 (vdd! 0) vsource dc=1.1V type=dc

//Cin is 0 for addition, 1 for subtraction

VCiAdd (inCiAdd 0) vsource dc=0V type=dc

VCiSub (inCiSub 0) vsource dc=1.1V type=dc

//V0 (inA0 0) vsource dc=0V type=dc

//V1 (inA1 0) vsource dc=0V type=dc

V2 (inA2 0) vsource dc=0V type=dc

V3 (inA3 0) vsource dc=0V type=dc

V4 (inA4 0) vsource dc=0V type=dc

V5 (inA5 0) vsource dc=0V type=dc

V6 (inA6 0) vsource dc=0V type=dc

V7 (inA7 0) vsource dc=0V type=dc

V8 (inA8 0) vsource dc=0V type=dc

V9 (inA9 0) vsource dc=0V type=dc

V10 (inA10 0) vsource dc=0V type=dc

V11 (inA11 0) vsource dc=0V type=dc

V12 (inA12 0) vsource dc=0V type=dc

V13 (inA13 0) vsource dc=0V type=dc

V14 (inA14 0) vsource dc=0V type=dc

V15 (inA15 0) vsource dc=0V type=dc

//V16 (inB0 0) vsource dc=0V type=dc

//V17 (inB1 0) vsource dc=0V type=dc

V18 (inB2 0) vsource dc=0V type=dc

V19 (inB3 0) vsource dc=0V type=dc

V20 (inB4 0) vsource dc=0V type=dc

V21 (inB5 0) vsource dc=0V type=dc

V22 (inB6 0) vsource dc=0V type=dc

V23 (inB7 0) vsource dc=0V type=dc

V24 (inB8 0) vsource dc=0V type=dc

V25 (inB9 0) vsource dc=0V type=dc

V26 (inB10 0) vsource dc=0V type=dc

V27 (inB11 0) vsource dc=0V type=dc

V28 (inB12 0) vsource dc=0V type=dc

V29 (inB13 0) vsource dc=0V type=dc

V30 (inB14 0) vsource dc=0V type=dc

V31 (inB15 0) vsource dc=0V type=dc

VINA0 (inA0 0) vsource val0=0 val1=1.1 period=1n delay=0 rise=0.01n fall=0.01n width=1n/2 type=pulse

VINA1 (inA1 0) vsource val0=0 val1=1.1 period=2n delay=0 rise=0.01n fall=0.01n width=2n/2 type=pulse

VINB0 (inB0 0) vsource val0=0 val1=1.1 period=4n delay=0 rise=0.01n fall=0.01n width=4n/2 type=pulse

VINB1 (inB1 0) vsource val0=0 val1=1.1 period=8n delay=0 rise=0.01n fall=0.01n width=8n/2 type=pulse

//VINB (inB 0) vsource val0=0 val1=1.1 period=2n delay=0 rise=0.01n fall=0.01n width=2n/2 type=pulse

//VINC (inCi 0) vsource val0=0 val1=1.1 period=4n delay=0 rise=0.01n fall=0.01n width=4n/2 type=pulse

1. Netlist for SHIFT

// Generated for: spectre

// Generated on: Apr 9 19:24:10 2012

// Design library name: Project

// Design cell name: Test\_16\_bit\_shifter

// Design view name: schematic

simulator lang=spectre

global 0 vdd!

parameters wp=360n wn=360n ln=50n lp=50n

include "/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_nom/NMOS\_VTL.inc"

include "/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_nom/PMOS\_VTL.inc"

// Library name: Project

// Cell name: 1\_bit\_Inverter

// View name: schematic

subckt Project\_1\_bit\_Inverter\_schematic VDD VSS in out

M0 (out in VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n \

pd=300n ld=105n ls=105n m=1

M1 (out in VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n \

pd=300n ld=105n ls=105n m=1

ends Project\_1\_bit\_Inverter\_schematic

// End of subcircuit definition.

// Library name: Project

// Cell name: 2:1\_MUX

// View name: schematic

subckt \_sub0 VDD VSS in0 in1 out sel0

M3 (net7 sel0 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M2 (out net45 net7 net7) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M1 (net15 net41 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M0 (out net49 net15 net15) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M7 (out net45 net28 net28) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M6 (out sel0 net28 net28) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M5 (net28 net49 VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

M4 (net28 net41 VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 \

ps=300n pd=300n ld=105n ls=105n m=1

I2 (VDD VSS sel0 net41) Project\_1\_bit\_Inverter\_schematic

I1 (VDD VSS in1 net45) Project\_1\_bit\_Inverter\_schematic

I0 (VDD VSS in0 net49) Project\_1\_bit\_Inverter\_schematic

ends \_sub0

// End of subcircuit definition.

// Library name: Project

// Cell name: 16\_bit\_shifter

// View name: schematic

subckt Project\_16\_bit\_shifter\_schematic VDD VSS in00 in01 in02 in03 in04 \

in05 in06 in07 in08 in09 in10 in11 in12 in13 in14 in15 out00 out01 \

out02 out03 out04 out05 out06 out07 out08 out09 out10 out11 out12 \

out13 out14 out15 sel0 sel1

I31 (VDD VSS VSS VSS out00 sel1) \_sub0

I30 (VDD VSS net205 VSS out01 sel1) \_sub0

I29 (VDD VSS net199 VSS out02 sel1) \_sub0

I28 (VDD VSS net193 net205 out03 sel1) \_sub0

I27 (VDD VSS net175 net163 out07 sel1) \_sub0

I26 (VDD VSS net169 net187 out06 sel1) \_sub0

I25 (VDD VSS net163 net193 out05 sel1) \_sub0

I24 (VDD VSS net187 net199 out04 sel1) \_sub0

I23 (VDD VSS net133 net121 out12 sel1) \_sub0

I22 (VDD VSS net157 net127 out13 sel1) \_sub0

I21 (VDD VSS net151 net133 out14 sel1) \_sub0

I20 (VDD VSS net145 net157 out15 sel1) \_sub0

I19 (VDD VSS net127 net115 out11 sel1) \_sub0

I18 (VDD VSS net121 net181 out10 sel1) \_sub0

I17 (VDD VSS net115 net175 out09 sel1) \_sub0

I16 (VDD VSS net181 net169 out08 sel1) \_sub0

I15 (VDD VSS in08 in07 net115 sel0) \_sub0

I14 (VDD VSS in09 in08 net121 sel0) \_sub0

I13 (VDD VSS in10 in09 net127 sel0) \_sub0

I12 (VDD VSS in11 in10 net133 sel0) \_sub0

I11 (VDD VSS in15 in14 net0334 sel0) \_sub0

I10 (VDD VSS in14 in13 net145 sel0) \_sub0

I9 (VDD VSS in13 in12 net151 sel0) \_sub0

I8 (VDD VSS in12 in11 net157 sel0) \_sub0

I7 (VDD VSS in04 in03 net163 sel0) \_sub0

I6 (VDD VSS in05 in04 net169 sel0) \_sub0

I5 (VDD VSS in06 in05 net175 sel0) \_sub0

I4 (VDD VSS in07 in06 net181 sel0) \_sub0

I3 (VDD VSS in03 in02 net187 sel0) \_sub0

I2 (VDD VSS in02 in01 net193 sel0) \_sub0

I1 (VDD VSS in01 in00 net199 sel0) \_sub0

I0 (VDD VSS in00 VSS net205 sel0) \_sub0

ends Project\_16\_bit\_shifter\_schematic

// End of subcircuit definition.

// Library name: Project

// Cell name: 16\_bit\_Inverter

// View name: schematic

subckt Project\_16\_bit\_Inverter\_schematic VDD VSS in00 in01 in02 in03 in04 \

in05 in06 in07 in08 in09 in10 in11 in12 in13 in14 in15 out00 out01 \

out02 out03 out04 out05 out06 out07 out08 out09 out10 out11 out12 \

out13 out14 out15

I5 (VDD VSS in01 out01) Project\_1\_bit\_Inverter\_schematic

I4 (VDD VSS in00 out00) Project\_1\_bit\_Inverter\_schematic

I7 (VDD VSS in03 out03) Project\_1\_bit\_Inverter\_schematic

I6 (VDD VSS in02 out02) Project\_1\_bit\_Inverter\_schematic

I19 (VDD VSS in15 out15) Project\_1\_bit\_Inverter\_schematic

I18 (VDD VSS in14 out14) Project\_1\_bit\_Inverter\_schematic

I17 (VDD VSS in13 out13) Project\_1\_bit\_Inverter\_schematic

I16 (VDD VSS in12 out12) Project\_1\_bit\_Inverter\_schematic

I12 (VDD VSS in08 out08) Project\_1\_bit\_Inverter\_schematic

I13 (VDD VSS in09 out09) Project\_1\_bit\_Inverter\_schematic

I14 (VDD VSS in10 out10) Project\_1\_bit\_Inverter\_schematic

I15 (VDD VSS in11 out11) Project\_1\_bit\_Inverter\_schematic

I8 (VDD VSS in04 out04) Project\_1\_bit\_Inverter\_schematic

I9 (VDD VSS in05 out05) Project\_1\_bit\_Inverter\_schematic

I10 (VDD VSS in06 out06) Project\_1\_bit\_Inverter\_schematic

I11 (VDD VSS in07 out07) Project\_1\_bit\_Inverter\_schematic

ends Project\_16\_bit\_Inverter\_schematic

// End of subcircuit definition.

// Library name: Project

// Cell name: 1\_bit\_InverterBuffer

// View name: schematic

subckt Project\_1\_bit\_InverterBuffer\_schematic VDD VSS in out

I1 (VDD VSS net11 out) Project\_1\_bit\_Inverter\_schematic

I0 (VDD VSS in net11) Project\_1\_bit\_Inverter\_schematic

ends Project\_1\_bit\_InverterBuffer\_schematic

// End of subcircuit definition.

// Library name: Project

// Cell name: 16\_bit\_InverterBuffer

// View name: schematic

subckt Project\_16\_bit\_InverterBuffer\_schematic VDD VSS in00 in01 in02 in03 \

in04 in05 in06 in07 in08 in09 in10 in11 in12 in13 in14 in15 out00 \

out01 out02 out03 out04 out05 out06 out07 out08 out09 out10 out11 \

out12 out13 out14 out15

I17 (VDD VSS in10 out10) Project\_1\_bit\_InverterBuffer\_schematic

I16 (VDD VSS in11 out11) Project\_1\_bit\_InverterBuffer\_schematic

I15 (VDD VSS in15 out15) Project\_1\_bit\_InverterBuffer\_schematic

I14 (VDD VSS in14 out14) Project\_1\_bit\_InverterBuffer\_schematic

I13 (VDD VSS in08 out08) Project\_1\_bit\_InverterBuffer\_schematic

I12 (VDD VSS in09 out09) Project\_1\_bit\_InverterBuffer\_schematic

I11 (VDD VSS in13 out13) Project\_1\_bit\_InverterBuffer\_schematic

I10 (VDD VSS in12 out12) Project\_1\_bit\_InverterBuffer\_schematic

I9 (VDD VSS in06 out06) Project\_1\_bit\_InverterBuffer\_schematic

I8 (VDD VSS in07 out07) Project\_1\_bit\_InverterBuffer\_schematic

I6 (VDD VSS in05 out05) Project\_1\_bit\_InverterBuffer\_schematic

I7 (VDD VSS in04 out04) Project\_1\_bit\_InverterBuffer\_schematic

I3 (VDD VSS in03 out03) Project\_1\_bit\_InverterBuffer\_schematic

I2 (VDD VSS in02 out02) Project\_1\_bit\_InverterBuffer\_schematic

I1 (VDD VSS in01 out01) Project\_1\_bit\_InverterBuffer\_schematic

I0 (VDD VSS in00 out00) Project\_1\_bit\_InverterBuffer\_schematic

ends Project\_16\_bit\_InverterBuffer\_schematic

// End of subcircuit definition.

// Library name: Project

// Cell name: Test\_16\_bit\_shifter

// View name: schematic

I0 (vdd! 0 net164 net165 net166 net167 net168 net169 net170 net171 net172 \

net173 net174 net175 net176 net177 net178 net179 out00 out01 out02 \

out03 out04 out05 out06 out07 out08 out09 out10 out11 out12 out13 \

out14 out15 net202 net198) Project\_16\_bit\_shifter\_schematic

I3 (vdd! 0 out00 out01 out02 out03 out04 out05 out06 out07 out08 out09 \

out10 out11 out12 out13 out14 out15 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 \

0) Project\_16\_bit\_Inverter\_schematic

I4 (vdd! 0 in00 in01 in02 in03 in04 in05 in06 in07 in08 in09 in10 in11 \

in12 in13 in14 in15 net164 net165 net166 net167 net168 net169 \

net170 net171 net172 net173 net174 net175 net176 net177 net178 \

net179) Project\_16\_bit\_InverterBuffer\_schematic

I6 (vdd! 0 sel1 net198) Project\_1\_bit\_InverterBuffer\_schematic

I5 (vdd! 0 sel0 net202) Project\_1\_bit\_InverterBuffer\_schematic

V0 (vdd! 0) vsource dc=1.1 type=dc

1. NETLIST FOR REGISTER

simulator lang=spectre

global 0 vdd!

include "/net/plato.ee.Virginia.EDU/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_ff/NMOS\_VTL.inc"

include "/net/plato.ee.Virginia.EDU/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_ff/PMOS\_VTL.inc"

// Cell name: ece3663Inverter

// An inverter with sizing parameters and parameterized AD,AS,PD,PS

// The S/D parameters assume a single-finger device

subckt ece3663Inverter VDD VSS in out

parameters wp=180n wn=90n mult=1

MP (out in VDD VDD) PMOS\_VTL w=wp l=50n as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

MN (out in VSS VSS) NMOS\_VTL w=wn l=50n as=100n\*wn ad=100n\*wn ps=200n+wn pd=200n+wn m=mult

ends ece3663Inverter

// End of subcircuit definition

// Cell name: master-slave positive edge triggered register

subckt MSposEdgeReg VDD VSS CLK D Q

parameters wp=180n wn=90n mult=1

I0 (VDD VSS net3 net0) ece3663Inverter

I1 (VDD VSS D net5) ece3663Inverter

I2 (VDD VSS net1 net3) ece3663Inverter

I3 (VDD VSS Q net9) ece3663Inverter

I4 (VDD VSS net3 net10) ece3663Inverter

I5 (VDD VSS net7 Q) ece3663Inverter

I6 (VDD VSS CLK net6) ece3663Inverter

P0 (net0 net6 net1 VDD) PMOS\_VTL w=wp l=50n as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

P1 (net5 CLK net1 VDD) PMOS\_VTL w=wp l=50n as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

P2 (net9 CLK net7 VDD) PMOS\_VTL w=wp l=50n as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

P3 (net10 net6 net7 VDD) PMOS\_VTL w=wp l=50n as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

N0 (net0 CLK net1 VSS) NMOS\_VTL w=wn l=50n as=100n\*wn ad=100n\*wn ps=200n+wn pd=200n+wn m=mult

N1 (net5 net6 net1 VSS) NMOS\_VTL w=wn l=50n as=100n\*wn ad=100n\*wn ps=200n+wn pd=200n+wn m=mult

N2 (net9 net6 net7 VSS) NMOS\_VTL w=wn l=50n as=100n\*wn ad=100n\*wn ps=200n+wn pd=200n+wn m=mult

N3 (net10 CLK net7 VSS) NMOS\_VTL w=wn l=50n as=100n\*wn ad=100n\*wn ps=200n+wn pd=200n+wn m=mult

ends MSposEdgeReg

// End of subcircuit definition

// Cell name: 8b register

subckt reg8b VDD VSS CLK D0 D1 D2 D3 D4 D5 D6 D7 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

parameters wp=180n wn=90n mult=1

I0 (VDD VSS CLK D0 Q0) MSposEdgeReg

I1 (VDD VSS CLK D1 Q1) MSposEdgeReg

I2 (VDD VSS CLK D2 Q2) MSposEdgeReg

I3 (VDD VSS CLK D3 Q3) MSposEdgeReg

I4 (VDD VSS CLK D4 Q4) MSposEdgeReg

I5 (VDD VSS CLK D5 Q5) MSposEdgeReg

I6 (VDD VSS CLK D6 Q6) MSposEdgeReg

I7 (VDD VSS CLK D7 Q7) MSposEdgeReg

ends reg8b

// End of subcircuit definition

// Cell name: 16b register

subckt reg16b VDD VSS CLK D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15

parameters wp=180n wn=90n mult=1

I0 (VDD VSS CLK D0 D1 D2 D3 D4 D5 D6 D7 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7) reg8b

I1 (VDD VSS CLK D8 D9 D10 D11 D12 D13 D14 D15 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15) reg8b

ends reg16b

// End of subcircuit definition

// instance of 16b register

I0 (vdd! 0 CLK D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15) reg16b

// stimuli

V0 (vdd! 0) vsource dc=1.1V type=dc

clock0 (CLK 0) vsource val0=0 val1=1.1 period=100p delay=25p rise=0.01p fall=0.01p width=50p type=pulse

data0 (D0 0) vsource val0=0 val1=1.1 period=200p delay=0 rise=0.01p fall=0.01p width=40p type=pulse

// data1 (D1 0) vsource val0=0 val1=1.1 period=80p delay=2p rise=0.01p fall=0.01p width=15p type=pulse

// data2 (D2 0) vsource val0=0 val1=1.1 period=80p delay=4p rise=0.01p fall=0.01p width=15p type=pulse

// data3 (D3 0) vsource val0=0 val1=1.1 period=80p delay=6p rise=0.01p fall=0.01p width=15p type=pulse

// data4 (D4 0) vsource val0=0 val1=1.1 period=80p delay=8p rise=0.01p fall=0.01p width=15p type=pulse

// data5 (D5 0) vsource val0=0 val1=1.1 period=80p delay=10p rise=0.01p fall=0.01p width=15p type=pulse

// data6 (D6 0) vsource val0=0 val1=1.1 period=80p delay=12p rise=0.01p fall=0.01p width=15p type=pulse

// data7 (D7 0) vsource val0=0 val1=1.1 period=80p delay=14p rise=0.01p fall=0.01p width=15p type=pulse

data8 (D8 0) vsource val0=0 val1=1.1 period=200p delay=0 rise=0.01p fall=0.01p width=40p type=pulse

// data9 (D9 0) vsource val0=0 val1=1.1 period=80p delay=18p rise=0.01p fall=0.01p width=15p type=pulse

// data10 (D10 0) vsource val0=0 val1=1.1 period=80p delay=20p rise=0.01p fall=0.01p width=15p type=pulse

// data11 (D11 0) vsource val0=0 val1=1.1 period=80p delay=22p rise=0.01p fall=0.01p width=15p type=pulse

// data12 (D12 0) vsource val0=0 val1=1.1 period=80p delay=24p rise=0.01p fall=0.01p width=15p type=pulse

// data13 (D13 0) vsource val0=0 val1=1.1 period=80p delay=26p rise=0.01p fall=0.01p width=15p type=pulse

// data14 (D14 0) vsource val0=0 val1=1.1 period=80p delay=28p rise=0.01p fall=0.01p width=15p type=pulse

// data15 (D15 0) vsource val0=0 val1=1.1 period=80p delay=30p rise=0.01p fall=0.01p width=15p type=pulse